## REMARKS

Claims 1-26 and 29-35 are all the claims pending in the application. Claims 8-15 and 22-26 have been withdrawn from consideration. Claims 1-7, 16-21, and 29-35 stand rejected.

***Claims Rejection - 35 U.S.C. § 102***

Claims 1, 3, 6-7, 29, 33 and 35 are rejected under 35 U.S.C. § 102(b) as allegedly being anticipated by Akiyama et al. (J.P 11-194316, hereinafter "Akiyama"). For at least the following reasons Applicant respectfully traverses the rejection.

Claim 1

Claim 1 recites in part:

> a first voltage supply and a second voltage supply which respectively supply a high level voltage signal and a low level voltage signal to a common electrode;
> ...
> wherein a high level of a signal passing through the at least one signal line is higher than the high level voltage signal supplied by said first voltage supply and a low level of the signal passing through the signal line is lower than the low level voltage signal supplied by said second voltage supply.

Accordingly, under the claim language the first voltage supply provides a high level voltage signal and the second voltage supply provides a low level signal. On page 3 of the Office Action, the Examiner alleges that +Vdd serves as the first voltage supply and -Vee serves as the second voltage supply. However, in response to the Applicant's argument that Akiyama fails to disclose that a high level of a signal passing through the at least one signal line (allegedly Vcom) is higher than the high level voltage signal supplied by said first voltage supply and a low level of the signal passing through the signal line is lower than the low level voltage signal (allegedly Vcom) supplied by said second voltage supply, the Examiner states that -Vee is the high level voltage supplied by the first voltage supply and +Vdd is the low level voltage signal

supplied by the second voltage supply. *See* Office Action, pg. 3. Applicant submits that the Examiner is inconsistent in his statements. Additionally, the Examiner is incorrect with regards to his assertions in page 3 of the Office Action. Specifically, as quoted above, with respect to the claimed language, in Akiyuma +Vdd must serve as the alleged first signal as it supplies a high level voltage signal and -Vee must serve as the alleged second signal as it supplies a low level voltage. However, there is no teaching that a high level of Vcom is higher then +Vdd or the lower level of Vcom is lower then -Vee. Accordingly, Applicant respectfully submits that claim 1 is allowable.

Furthermore, with reference to the 7th and 8th paragraph of the Office Action regarding claim 1, Applicants submit that even though "at least one signal line" in claim 1 allegedly correspond to "VCOM" in the cited reference Akiyama and the "first transistor" and the "second transistor" in claim 1 allegedly correspond to "TR1 or TR3" and "TR2 or TR4" in the cited reference Akiyama, as interpreted by the examiner and shown in FIG. 6 of the cited reference Akiyama, **"VCOM" is not connected to the gate terminals of "TR1, TR2, TR3 and "TR4**." Therefore, the cited reference Akiyama is inconsistent with the description which reads "at least one signal line is **connected to the gate terminals** of a first transistor and a second transistor" in claim 1 of the present application. That is, since VCOM is **not at all connected to the gate** terminals of the alleged first and second transistors, it is improper for the Examiner to assert that Akiyama teaches this unique feature of claim 1.

Claim 33

Claim 33 contains features similar to the features of claim 1. Accordingly, it is believed to be allowable for analogous reasons.

Dependent Claims 3, 6-7, 29 and 35

Dependent claims 3, 6-7, 29 and 35 are believed to be allowable at least by virtue of their dependency on independent claim 1.

With regard to claim 3, Applicants submit that VCOM in FIG. 6 of the cited reference Akiyama, which was allegedly regarded as the "common signal lines" by the examiner, **is not connected to the gate terminals** of the P-type first transistor TR1 or TR3 or the N-type second transistor TR2 or TR4. Therefore, claim 3 distinguishes from the cited reference Akiyama.

With regard to claim 6, Applicants respectfully submit that the cited reference Akiyama describes in Paragraph [0012] that a pixel transistor is a TFT 24, but it does not describe that **the transistor of a VCOM drive circuit is a TFT**.

With regard to claim 29, Applicants respectfully submit that paragraph [0014] of the cited reference Akiyama describes that the X driver 12 includes a D/A converter which converts the gradation data into an analog signal voltage level. However, it does not include **a level shift circuit** that inputs a high/low logic signal and outputs a logic signal with an enlarged amplitude.

***Claim Rejections - 35 U.S.C. § 103***

Claims 2, 16-21, 30-32 are rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over Akiyama in view of Hosokawa et al. (US Patent No: 4,393,380, hereinafter "Hosokawa").

Claims 4-5 are rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over Akiyama in view of Taki (U.S. 2002/000833, hereinafter "Taki")

Claims 19-20, 32, are rejected under 35 U.S.C. § 103(a) as being unpatentable over Akiyama in view of Hosokawa and Taki.

Independent claim 34 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Akiyama in view of Taki (U.S. 6,329,834).

Applicant respectfully traverses these rejections for at least the following reasons.

Claims 2 and 16

Hosokawa fails to make up for the deficiencies of Akiyama with respect to claim 1. Therefore, claim 2 and 16 are believed to be allowable at least by virtue of its dependency on independent claim 1.

Dependent claims 4, 5 and 30

Taki fails to make up for the deficiencies of Akiyama with respect to features of claim 1. Accordingly, claims 4, 5 and 30 are believed to be allowable at least by virtue of their dependency on independent claim 1.

With regard to claim 4, Applicants submit that the Examiner regards "said one signal line" as VCOM in FIG. 6 of the cited reference Akiyama, but VCOM is not connected to the gate terminal of the first transistor TR1 or TR3 or the second transistor TR2 or TR4. In addition, in FIG. lb of the cited reference Taki the P-type transistor and the N-type transistor are serially connected and are not connected in parallel. Furthermore, it does not describe that the high potential of a signal inputted to the gate terminal A of the transistor is higher than VDD and the low potential is lower than GND.

With regard to claim 5, Applicants submit that the cited reference Akiyama does not describe that the potential of VCOM, which the examiner regards as "one signal line," is the potential (VON, VOFF) of the voltage supply of the gate driver 14.

Furthermore, claim 30 is patentable at least for reasons discussed above with respect to claim 29.

Dependent Claim 17

Claim 17 is patentable at least for reasons discussed above with respect to claim 1. Claim 17 is also patentable at least by virtue of its dependency.

Dependent Claims 18-21 and 31-32

Taki and Hosakawa fail to make up for the deficiencies of Akiyama. Therefore, claims 18-21 and 31-32 are believed to be allowable at least by virtue of their dependency on claim 17.

Furthermore, claim 18 is patentable at least for reasons discussed above with respect to claim 3.

Furthermore, claim 19 is patentable at least for reasons discussed above with respect to claim 4.

Furthermore, claim 20 is patentable at least for reasons discussed above with respect to claim 5.

Furthermore, claim 21 is patentable at least for reasons discussed above with respect to claim 6.

Furthermore, claim 31 and 32 are patentable at least for reasons discussed above with respect to claim 29.

Independent Claim 34

Claim 34 contains features similar to claim 1. Accordingly, it is allowable for analogous reasons as Taki (U.S. 6,329,834) fails to make up for the deficiencies of Akiyama with respect to features of claim 1.

Specifically, in FIG. 19 of the cited reference Taki, one signal line 38 connected to the gate terminals of transistors 45 and 50 is generated by a circuit 1. Therefore, the level of voltage through the signal line 38 is limited to either a high level voltage VDD or a low level voltage GND. In other words, the level of voltage that can be obtained by the signal line 38 exceeds neither the voltage VDD of a first voltage supply nor the voltage GND of a second voltage supply in a circuit 2.

On the other hand, the claimed invention describes that the high level of voltage (COMD) through a signal line is higher than the voltage (VCOMH) of the first voltage supply and the low level of voltage (COMD) through the signal line is lower than the voltage (VCOML) of the second voltage supply.

Additionally, the electrode drive circuit of Akiyama requires the presence of elements present between the voltage source and the terminal of the respective transistors. Applicant respectfully notes that that "[i]f the proposed modification or combination of the prior art would change the principle of operation of the prior art invention being modified, the teachings of the references are not sufficient to render the claims prima facie obvious. In re Ratti, 270 F.2d 810, 123 USPQ 349 (CCPA 1959)." MPEP at § 2143.01(VI). Here, any modification of Akiyama so that there is a direct connection between the respective voltage supplies and respective terminals of the transistors as recited in the claim language, would change the principle of operation of Akiyama. Accordingly, claim 34 is allowable for this additional reason.

***Conclusion***

In view of the above, reconsideration and allowance of this application are now believed to be in order, and such actions are hereby solicited. If any points remain in issue which the

Examiner feels may be best resolved through a personal or telephone interview, the Examiner is kindly requested to contact the undersigned at the telephone number listed below.

The USPTO is directed and authorized to charge all required fees, except for the Issue Fee and the Publication Fee, to Deposit Account No. 19-4880. Please also credit any overpayments to said Deposit Account.

Respectfully submitted,

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Date: October 17, 2008